UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/827,239	04/20/2004	Edward J.W. Whittaker	115-37US/12667/100122	2542

23838 7590 07/13/2005

KENYON & KENYON
1500 K STREET NW
SUITE 700
WASHINGTON, DC 20005

EXAMINER	
ENGLUND, TERRY LEE	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 07/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/827,239	WHITTAKER, EDWARD J.W.	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04202004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: Fig. 2 lacks "R1" (e.g. see page 5, line 1, and page 6, line 12); Fig. 3 lacks "R1" (e.g. see page 6, line 8 of paragraph 0022; and page 7, line 14 of paragraph 0024); and neither Fig. 4a nor 4b shows "406" (e.g. see page 10, line 1 of paragraph 0034). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to because Fig. 2 indicates "206" is the line coupled between M3 and the bases of transistors Q1/Q2. However, page 5, line 1 of paragraph 0019 identifies "206" with "current ratioing circuit." Therefore, it is suggested the "206" shown in Fig. 2 be modified to more clearly indicate what it actually relates to. "Q3" of Fig. 3 should be --C1-- (e.g. see page 6, lines 8-9 of paragraph 0022, and page 8, lines 1 and 7 of paragraph 0025). Similar to Fig. 2's "206", Fig. 3 shows "306" going to the line (or node) coupled in common to resistors R2-R4. However, the first line of paragraph 0024 on page 7 identifies "306" as a "current

ratioing circuit." Therefore, it is suggested Fig. 3's "306" be shown more clearly to indicate what it actually relates to.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The applicant is reminded of the proper language for an abstract of the disclosure. For example, it should avoid using phrases or terms that can be implied, such as, "novel" and "is disclosed." It is understood that a patent's abstract summarizes an invention that is disclosed, and since it is an invention, it should be novel. Therefore the following changes are suggested: 1) delete the use of "novel" in lines 1, 4, and 6; and 2) on line 1, delete "is disclosed. The circuit" to remove the "is disclosed" phrase, and to combine the first and sentences into a single sentence.

The abstract of the disclosure is objected to because "used" on line 5 should be --use-- to improve word flow. Also, since the circuit had been previously described in the abstract, it is suggested "A" on line 6 be changed to --The--. Corrections are required. See MPEP § 608.01(b).

The disclosure is objected to because of the following informalities: Page 6, last line of paragraph 0020 should have --213-- instead of "312." Page 5, first line of paragraph 0019 should have the second occurrence of "circuit" deleted. Page 7, first line of paragraph 0024 should have the second occurrence of "circuit" deleted. The current mirror ports on lines 2 and 10 of paragraph 0024 do not correspond to the ports on lines 7-8 of paragraph 0023. For example, line 2 of paragraph 0024 identifies "305b" with the first current mirror port, but line 8 of paragraph 0023 relates it to the second current mirror port. Therefore, it is suggested changes be made to provide consistent labeling throughout the disclosure. Page 8, line 5 of paragraph 0026 should have --1-- instead of "1a" since only "Fig. 1" is shown. It is suggested the phrase "the PNP transistors are used in order" be changed to --PNP transistors can be used-- on page 9, first line of paragraph 0030. The first and/or second current mirror ports cited in paragraphs 0034-0036 of pages 10-11 do not appear to correspond to the first/second current mirror ports described in paragraph 0033, and with what is shown within Figs. 4a and 4b. For example, it is believed the "first current mirror port 405b" of paragraph 0034 (line 2) is actually referring to the --second current mirror port 405b-- (e.g. see the last two lines of paragraph 0033). Therefore, it is suggested the use of the "first" and "second" current mirror ports, along with their corresponding reference designator "405b" or "405a" be carefully reviewed and considered within paragraphs 0033 (lines 7-8), 0034 (lines 2 and 10), 0035 (lines 8-9), and 0036 (line 2). Appropriate changes should be made to ensure the ports are identified consistently throughout the disclosure. [Note:

Other than identifying current mirror 405 with "first", and that FETs M1 and M2 are PFETs, paragraph 0035 replicates paragraph 0033. Therefore, it is suggested one of these paragraphs be deleted to minimize duplicate type descriptions.] To correspond to the reference designators shown in Figs. 4a and 4b, "400 and fourth 450" on line 3 of paragraph 0032 (page 10) should be --450 and fourth 400--. Page 10, first line of paragraph 0034 should have the second occurrence of "circuit" deleted. Page 11, line 5 of paragraph 0037 should have --1-- instead of "1a" since only "Fig. 1" is shown. It is not clear what "because of by the" means on page 13, line 2 of paragraph 0040. For example, was --because the-- meant? Page 11, paragraph 0036 should have "432" on line 4 changed to --433--, and "source" on line 7 changed to --drain-- to accurately correspond to what is shown within Figs. 4a and 4b. Related to the same type of labeling as previously described, it is not clear if "the first...405b" on line 5 of paragraph 0038 (page 12) refers back to "the first...405a" cited in paragraph 0033, or to "the first...405b" cited in paragraph 0035. Line 7 of paragraph 0039, on page 12, should have --seventh and sixth-- instead of "first and second" (e.g. see line 4 of the same paragraph). To correspond to the third embodiment shown in Fig. 4a with "450", "400" should be changed to --450-- on pages 13 (line 1 of paragraph 0041, and line 4 of paragraph 0043); and 14 (line 1 of paragraph 0044). For similar reasons, both occurrences of "450" on the second line of paragraph 0044 should be changed to --400--; and "400 and "450" on the first line of both paragraphs 0045 and 0046 should be changed to --450 and 400--. However, if the applicant does not want to make all the changes in the disclosure with respect to "400" and "450", then those reference designators shown within Figs. 4a and 4b would need to be reversed. It is suggested the phrase "the PNP transistors are used in order" be changed to --PNP transistors can be used-- on page 15, first line

of paragraph 0047. Since claim 16 already recites "one of the...terminals", it is suggested claim 17 has --the-- added prior to "one" on line 5. Appropriate corrections are required.

Claim Objections

Claims 1-17 are objected to because of the following informalities: To minimize possible confusion with respect to the various ports, and to provide consistent labeling throughout the claims, it is suggested --current mirror-- be added after "second" on line 2 of claim 2. Claim 5, line 2 should have "transistor" changed to --transistors--; and "terminal" on both lines 5 and 6 changed to --terminals--. These changes will relate the presently recited single transistor (or terminal) back to its corresponding "plurality." Claim 7, line 4 should have --the-- added prior to "current between" to relate the current back to the "propagating current" of claim 6. Since the current mirror circuit of claim 1 already comprises the first/second current mirror ports, it is suggested --further-- be added prior to "comprises" on line 1 of both claims 8 and 9. To help distinguish between the two "a PFET" phrases in claim 10, it is suggested the second phrase be changed to --another PFET-- or --a second PFET--. Claim 16, line 2 "series first" should be changed to --series between the first-- to improve word flow, and to provide a clearer description of what is believed to be recited. Dependent claims carry over any objection(s) from any claim(s) upon which they depend. Appropriate corrections are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant

regards as the invention. Neither of the independent claims (i.e. 1 and 18) recites what "N" and "M" actually represent. For example, they could be (positive or negative) integers, fractions, or even equal to one another (e.g. N = 1 = M). In this latter example, the final output current would be equal to the input current, after being amplified with a gain of one. The use of "third" (i.e. "third field effect transistor", "third gate", "third drain", and "third source") in claim 7 implies first and second corresponding elements that have not been identified within the claim's chain of dependency. Similarly, the use of "second" in claim 8 implies a first that has not been identified within the claim's chain of dependency. For example, was claim 8 meant to depend on claim 9, which actually cites "a first FET"? The use of "second current source" in claim 11 implies a first one that has not been identified within the claim's chain of dependency. The phrase "between the third source and third gate terminals" on line 2 of claim 13 is misleading and/or inaccurate. For example, was --drain-- meant instead of "source" (e.g. see capacitor 341 and transistor 313 in the applicant's Fig. 3)? Claim 13's use of "second resistor" on line 4 implies a first resistor that has not been identified within the claim's chain of dependency. It is not clear what "the and M times N times the input current" means in claim 20. The inconsistent labeling of claim 18's portions is confusing. For example, how do the "first portion" and "second portion" on line 3 relate to the "first mirror portion" and "second mirror portion" on lines 2-3, and to the "first and second portion" on line 4? To minimize confusion, and help clarify what is actually being recited, it is suggested each reference to "first portion" (e.g. lines 2, 3, 4, 6, and 9), and each reference to "second portion" (e.g. lines 3, 4-5, 6, and 11) be changed to clearly identify each portion as being either a mirror portion, or a --ratioing portion--.

Claim 11 recites the limitation "the first and second base terminals of the first and second bipolar transistors" in lines 1-2. There is insufficient antecedent basis for these limitations in the claim. For example, was claim 11 meant to depend on claim 4, which cites a second bipolar transistor, wherein that claim depends on claim 3, which cites a first bipolar transistor?

Similar to claim 11 above, claim 12 recites the limitation "the second collector and second emitter terminals" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Dependent claims carry over any rejection(s) from any claim(s) upon which they depend.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-2, 8, and 18-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Min. Min's Fig. 2 shows a circuit comprising first supply voltage port Vcc; second supply voltage port (unlabeled ground); current mirror circuit MP4,MP5 having a first current mirror port (e.g. drain of MP5), and a second current mirror port (e.g. drain of MP4) for effectively propagating an input current from first supply voltage port Vcc (e.g. via R4,Q10,MN8,MN9) to the second supply port, wherein the first current mirror port provides N times the input current (N = 1; see column 3, lines 36-38); and current ratioing circuit MN10,MN5,20 comprising first

portion MN10 disposed between the first current mirror port (e.g. drain of MP5) and the second supply voltage port, and second portion MN5,20 disposed between first supply voltage port Vcc and ground. The second portion comprises load current path 20, and the current ratioing circuit propagates M times N times the input current through the load current path (M = N = 1; see column 3, lines 36-38). For example, input current Ibias through MN8 is equal to load current Ibias through 20,MN5. Therefore, claim 1 is anticipated. MN9 is one type of a current sink coupled between the second supply voltage port and the second current mirror port (drain of MP4). It effectively sinks input current Ibias through the current mirror circuit from the second current mirror port to the second supply voltage port, thus anticipating claim 2. The current mirror circuit comprises second FET MP4 with its second gate terminal, and its second drain and source terminals disposed in series between the first supply voltage port and the second current mirror port. Therefore, claim 8 is anticipated. Interpreting Min's Fig. 2 in a different manner, current mirror circuit MP4,MP5 is provided with first mirror portion MP5 and second mirror portion MP4, wherein first mirror portion MP5 propagates N times (N = 1; see column 3, lines 36-38) more current than second mirror portion MP4; current ratioing circuit MN10,MN5 is provided with first portion MN10 and second portion MN5 wherein second portion MN5 propagates M times (M = 1; see column 3, lines 36-38) more current than first portion MN10; input current Ibias (via MN8,MN9) is propagated through second mirror portion MP4; this input current is mirrored in first mirror portion MP5 to provide N times more current to the current ratioing circuit; the N times input current is ratioed to propagate through first portion MN10, and M times N times the input current is propagated through second portion MN5,20, anticipating claim 18. First voltage supply port Vcc is provided, and it is coupled directly to current mirror

circuit MP4,MP5, and to the current ratioing circuit via MP5 and 20. Due to the current mirror relationships within the circuit, and understood by one of ordinary skill in the art, a controlled current flow path is between the first voltage supply port and the first/second portions of the current ratioing circuit. This anticipates claim 19. Load 20 is coupled with the current ratioing circuit, and propagates the M times N times input current (i.e. 1 x 1 x Ibias), anticipating claim 20.

Claims 1-3, 8-10, and 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Aude et al. (Aude). Fig. 1 of Aude shows a circuit comprising first supply voltage port VDD; second supply voltage port Ground; current mirror circuit M1-M4 comprising first current mirror port (drain of M1) with current NxIref, and second current mirror port (drain of M2) with input current Iref; and current ratioing circuit X1-X2,Lload comprising first portion X1 between the first current mirror port and the second supply voltage port, and second portion X2 disposed between the first/second supply voltage ports, wherein the second portion comprises load current path Lload, and the current ratioing circuit propagates MxNxIref through the load current path. Therefore, claim 1 is anticipated. [Note: Aude's M1, M2, M3/M4, Cgd, X1, X2, R2/R1, Irefs, Vin, Ccoupling, and Lload closely correspond to M1, M2, M3, 341, Q1, Q2, R2, Iin, RF input, C2, and LOAD, respectively shown in the applicant's own Fig. 3.] Current sink Irefs is coupled between the second supply voltage port and the second current mirror port to sink input current Iref, anticipating claim 2. First portion X1 comprises first bipolar transistor X1 having a first base terminal; a first collector terminal coupled to the first current mirror port; and a first emitter coupled to the second supply voltage port. This anticipates claim 3. Since second FET M2 has a second gate terminal, and its second source and drain terminals are disposed in series between

the first supply voltage port and the second current mirror port, claim 8 is anticipated. First FET M1 has its first gate terminal coupled to the first drain terminal, and its first drain and source terminals disposed in series between the first supply voltage port and the first current mirror port. Since first FET is N times wider (i.e. NxW1/L1) than second FET M2, claim 9 is anticipated. First/second FETs M1/M2 are both PFETs, anticipating claim 10. Interpreting Aude's Fig. 1 differently, current mirror circuit M1,M2 is provided with first mirror portion M1 propagating N times more current (i.e. NxIref) than second mirror portion M2; current ratioing circuit X1,X2 is provided with first ratioing portion X1, and second ratioing portion X2 which propagates M times more current (i.e. MxNxIref) than first ratioing portion X1; Irefs propagates input current Iref through second mirror portion M2; current mirror circuit M1,M2 allows input current Iref to be mirrored in first mirror portion M1 to provide N times the input current (i.e. NxIref); X1 receives that current; and current ratioing circuit X1,X2 ratios NxIref to propagate through first mirror portion M1/first ratioing portion X1, and MxNxIref to propagate through second ratioing portion X2. These steps, and known current mirror relationships, anticipate claim 18. First voltage supply port VDD is provided, and is coupled directly to current mirror circuit M1,M2, and indirectly (via M1, M3, M4, and Lload) to the current ratioing circuit. Since M1-M4, and Lload provide a controlled current flow path between first voltage supply port VDD and first/ second ratioing portions X1/X2 of current ratioing circuit X1,X2, claim 19 is anticipated. Load Lload is provided coupled to the current ratioing circuit, and it has MxNxIref propagated through it, anticipating claim 20.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4-7, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aude et al. (Aude) as applied to claim 3 above. Although the reference of Aude shows/discloses a circuit comprising a current mirror circuit and a current ratioing circuit as previously described, Fig. 1 does not show the base terminals of X1 and X2 coupled together. Column 4, lines 20-24 disclose that equal voltages are applied to the bases of X1 and X2. Therefore, it would have been obvious to one of ordinary skill in the art to remove either M3 and R2, or M4 and R1 from Aude's circuit, wherein after one of these transistor/resistor sets is removed, the bases of X1 and X2 would be coupled together to ensure they would still receive the same voltage. In such a configuration, the second base terminal of second bipolar transistor X2 would be coupled to the first base terminal; the second collector terminal would be coupled to load current path Lload; and second emitter terminal could be coupled to second supply voltage port Ground. Since X2 is "M", and X1 is "1", it is understood second bipolar transistor X2 is M times larger than first bipolar transistor X1, and claim 4 is rendered obvious. By removing either transistor/resistor set M3/R2 or M4/R1, the number of components within the circuit is reduced, allowing the circuit to be reduced in size, while still providing equal voltages to be applied to the bases of the transistors X1,X2. Aude discloses that second bipolar transistor X2 can be a plurality of parallel connected transistors (e.g. see column 3, lines 20-28). Therefore, by applying the same type of

reasoning as described above with respect to claim 4, claim 5 is also rendered obvious. After one of the transistor/resistor sets M3/R2 and M4,R1 is removed as described above, the other set will comprise a current path disposed between first supply voltage port VDD and the coupled first/second base terminals. This current path will propagate current in response to input current Iref, rendering claim 6 obvious. With transistor/resistor set M3/R2 removed, and the lower terminal of R1 coupled to the base terminals of both X1 and X2, the current path comprises third FET M3 with its third gate terminal coupled to the second current mirror port (i.e. drain of M2), and its third drain/source terminals disposed in series along the current path. Therefore, the current propagation between the third source/drain terminals will be in dependence upon input current Iref, and claim 7 is rendered obvious. Capacitance Cgd can be considered one type of a loop stabilization circuit comprising first capacitor Cgd disposed between the third drain and gate terminals of third FET M4, and (second) resistor R1 is disposed between the third drain terminal and a node formed when the first/second base terminals are coupled together (to receive the same voltage). Capacitor Cgd and resistor R1 thus render claim 13 obvious.

No claim is allowable as presently written.

Allowable Subject Matter

However, claims 11-12, and 14-17 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. There is presently no motivation to modify or combine any prior art reference(s) to ensure: 1) a second current source is coupled to the first/second base terminals to provide an offset current as recited within claim 11 (upon which claims 12, and 15 depend); 2) the circuit also includes the third/fourth resistors disposed

between the first base terminal and node/second base terminal and node, as recited within claim 14; 3) the load current path comprises a differential amplification stage as recited within claim 16; or 4) the first/second bias ports of a differential amplification stage are each coupled to one of the third drain/source terminals of the third FET as recited within claim 17.

Prior Art

The other prior art references cited on the accompanying PTO-892 are deemed relevant to at least sections of the claimed invention. Although not used in any formal rejections described above, the references of Giuroiu and Tanase both show circuits comprising a current mirror circuit and a current ratioing current circuit. [Note: Since one of ordinary skill in the art understands a current mirror configured circuit provides an output that is some type of a multiple of its input current (e.g. the multiple can be unity, an integer (e.g. 2), or fraction (e.g. ½)), depending on the sizing of the transistors comprising the current mirror circuit, it will be understood the current mirror's output current will represent N times its input current.] Fig. 7C of Giuroiu shows current mirror circuit 310,315 receiving an input current (from 305) at mirror portion 310, and providing a corresponding N times the input current from mirror portion 315 to portion 255 of current ratioing circuit 255,260, wherein portion 260 provides a corresponding M times N times the input current to load current path 105,110. [Also noted in Giuroiu's Fig. 7C: The first/second biasing inputs of load current path/differential amplifier 105,110 are both coupled to the drain terminal of third FET 330.] Fig. 6 of Tanase shows mirror portion P1 of current mirror circuit P1,P3 receiving input current I; mirror portion P3 outputting (Mp)I to an unlabelled portion of a current ratioing circuit, which provides M_P*M_N*I from a corresponding unlabelled output portion. Therefore, both of these references should be carefully reviewed and

considered with respect to the broadest reasonable interpretation of the prior art references, and the claimed limitations.

The reference cited on the IDS submitted Apr 20, 2004 was reviewed and considered. It corresponds to the applicant's own Prior Art Fig. 1. It does not clearly show a first portion, of a current ratioing circuit, disposed between the first current mirror port (of a current mirror circuit) and a second supply voltage port as recited within the claims.

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund
29 Jun 2005

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800